A Brief Description of Gate and Delay Generators

Timothy Hoagland

December 2, 2004

Gate and delay generator provide two important elements in a data acquisition setup. First is the delay element, allowing an experimenter to delay a logic signal until it is needed. The second element is the gate, which can be used to select a time of interest. Both are essential for many data acquisition setups.

Delaying a logic pulse is often useful to compensate for intrinsic delays elsewhere in the system, such as cable delay or electronics delay. Most gate and delay generators provide both a course and fine delay adjustment.

The gate aspect of a gate and delay generator allows for an extended logic pulse. When a gate is triggered the module emits a logic pulse held in the "true" position longer than a traditional logic pulse. This provides an effective way of windowing an event. For example if you are using a computer to record a signal and you took data continuously you would use a lot of disk space. However you used a gate and delay generator and set a gate to occur around the interesting part of the signal then your computer would only take data when the gate is "true" and you would be able to store a lot more interesting data in the same disk space. Gate and Delay generators have adjustments to determine how long a gate should be.

Many gate and delay generators can also be run in latched mode, this means that the gate is started when it receives a signal and will continue to hold as "true" until a stop signal is received. This is useful to acknowledge signals.

It is important to note that a gate and delay generator looks at gates as long logic pulses. This means that you can use it to create delayed gates, which is often how they are used.

This is intended only as a general introduction to gate and delay generators and should not be relied upon to heavily for any particular setup since obviously the specifics of a particular gate and delay generator will depend on the model and manufacturer.

If you feel that something important has been left out here please contact **daqdocs@nscl.msu.edu**.